**T.E.S.S. Data Sheet**

Table of Contents

[Overview 3](#_Toc437936933)

[Features 3](#_Toc437936934)

[Abbreviations 3](#_Toc437936935)

[Block Diagram 4](#_Toc437936936)

[Layout 4](#_Toc437936937)

[Pin Layout 5](#_Toc437936938)

[Pin Table 5](#_Toc437936939)

[Data path 8](#_Toc437936940)

[Core 8](#_Toc437936941)

[Audio 8](#_Toc437936942)

[VGA 8](#_Toc437936943)

[Memory Map 8](#_Toc437936944)

[Peripheral interface 8](#_Toc437936945)

[Application 9](#_Toc437936946)

[Package Dimensions 9](#_Toc437936947)

[Verilog 9](#_Toc437936948)

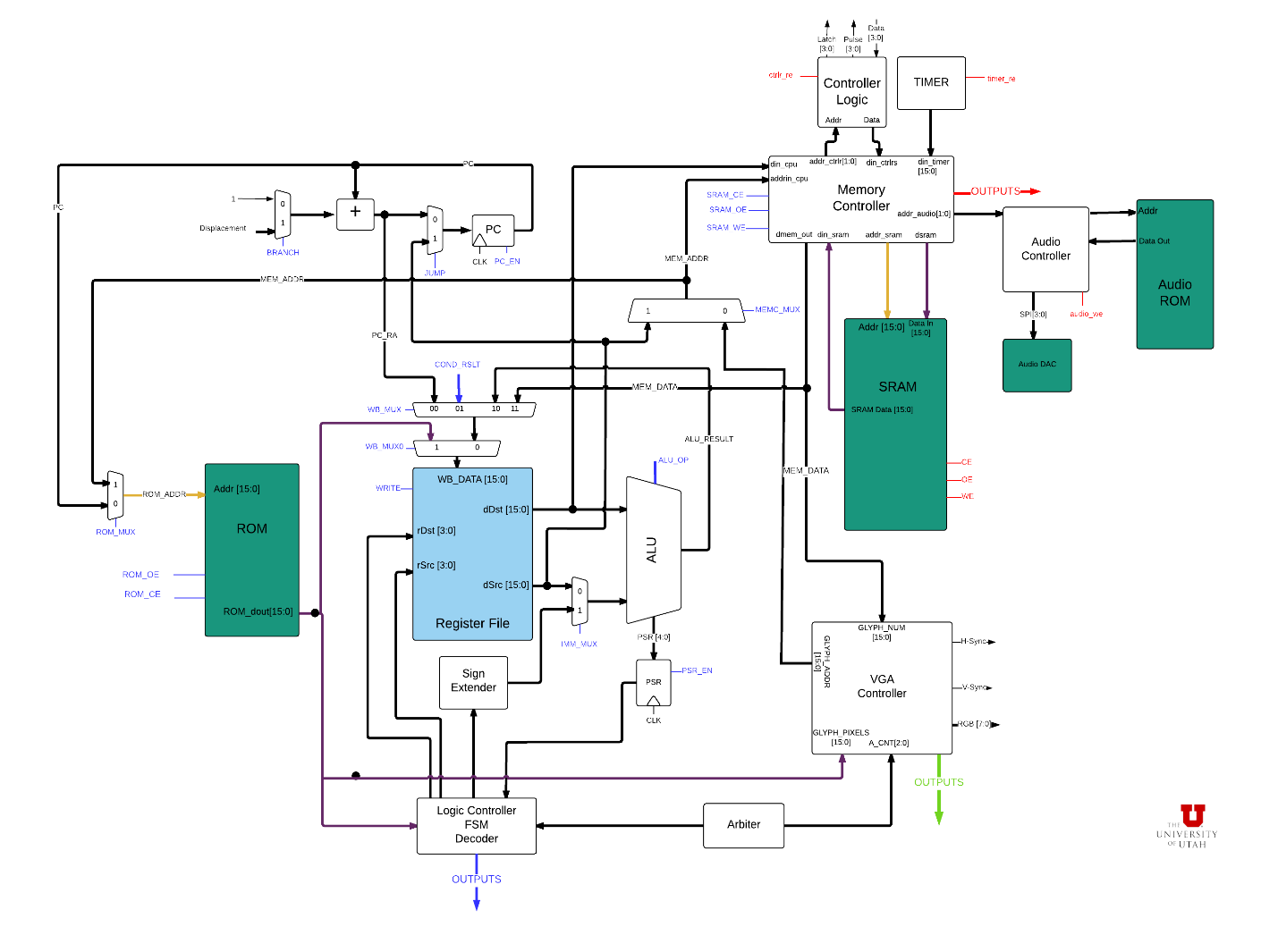
OverviewThe Titan Entertainment Super System (T.E.S.S) is a 16-bit microprocessor modeled after the CR16 architecture. With that being said, both its data path, and instruction set architecture (I.S.A) are very similar, but not identical to that of the CR16. The design also includes a sample-based audio playback system, as well as a 2-bit video graphics array (V.G.A) controller.  
  
An important feature of this integrated circuit (I.C) to note is that the memory needed to function needs to be supplied from off-chip memory I.C.’s . The specifications required for each memory I.C. is discussed in section 7.  
  
The T.E.S.S. was designed with the specific category of simple video games in mind. However the core was designed to be able to run a wide variety of applications. It is important to note that due to the memory I.C.’s being easily interchangeable, it easy to run several different applications, as long as they adhere to the I.S.A. discussed in later sections.

# Features

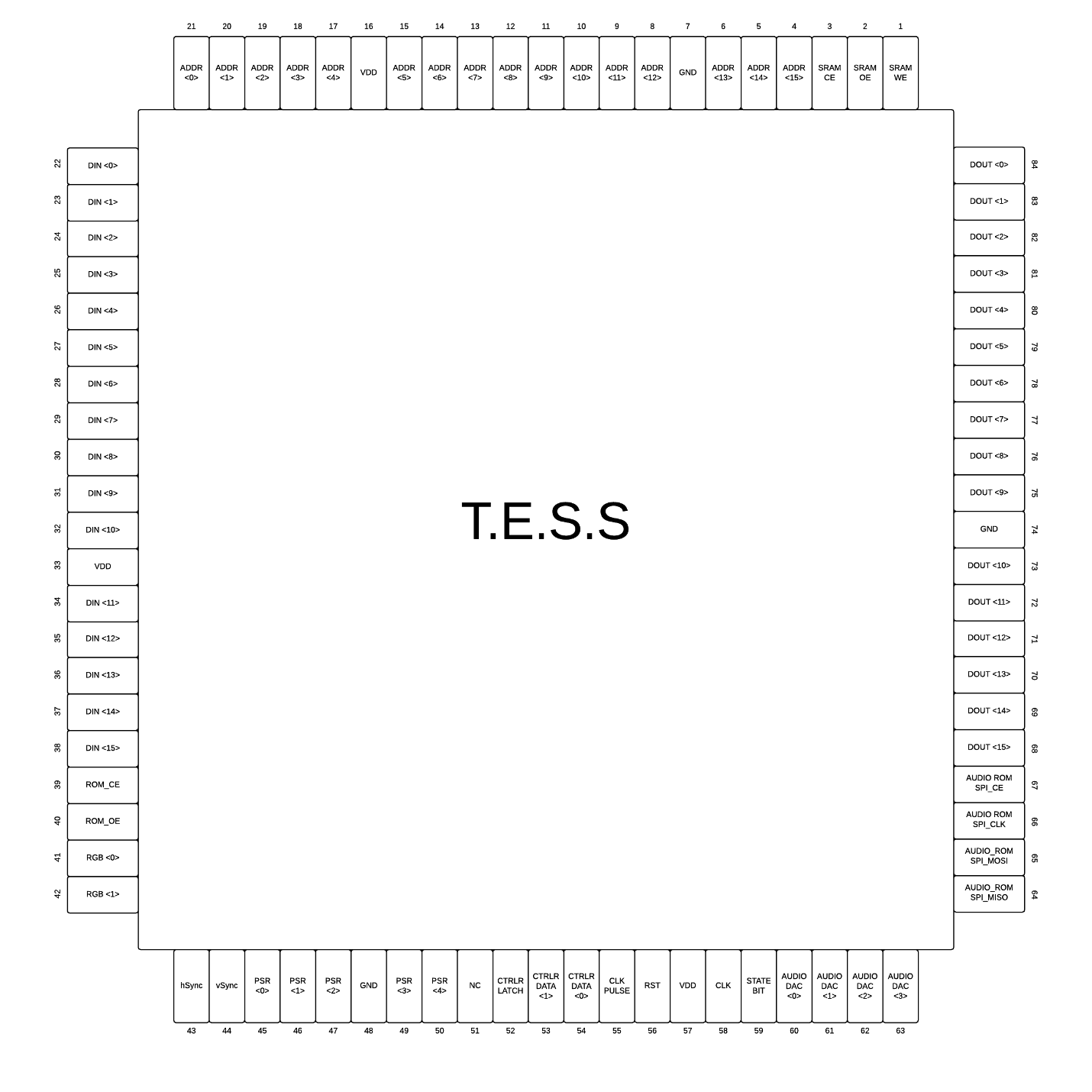
* 16-bit data path
* 2-bit VGA
* Sample-based audio playback
* 12.5 MHz clock speed
* General purpose

# Abbreviations

|  |  |
| --- | --- |
| Abbreviation | Meaning |
| ISA | Instruction Set Architecture |
| TESS | Titan Entertainment Super System |
| VGA | Video Graphics Array |
| IC | Integrated Circuit |
| ALU | Arithmetic Logic Unit |
| SRAM | Static Random Access Memory |
| ROM | Read Only Memory |
| SPI | Serial Peripheral Interface |
| PC | Program Counter |
| DAC | Digital-to-Analog Converter |
| FSM | Finite State Machine |

Block Diagram

Layout

Pin Layout

# Pin Table

|  |  |  |
| --- | --- | --- |
| Name | Number | Description |
| SRAM WE | 1 | SRAM Write Enable |
| SRAM OE | 2 | SRAM Output Enable |
| SRAM CE | 3 | SRAM Chip Enable |
| ADDR <15> | 4 | Address Bit-15 connected to both SRAM and ROM |
| ADDR <14> | 5 | Address Bit-14 connected to both SRAM and ROM |
| ADDR <13> | 6 | Address Bit-13 connected to both SRAM and ROM |
| GND | 7 | Ground |
| ADDR <12> | 8 | Address Bit-12 connected to both SRAM and ROM |
| ADDR <11> | 9 | Address Bit-11 connected to both SRAM and ROM |
| ADDR <10> | 10 | Address Bit-10 connected to both SRAM and ROM |
| ADDR <9> | 11 | Address Bit-9 connected to both SRAM and ROM |
| ADDR <8> | 12 | Address Bit-8 connected to both SRAM and ROM |
| ADDR <7> | 13 | Address Bit-7 connected to both SRAM and ROM |
| ADDR <6> | 14 | Address Bit-6 connected to both SRAM and ROM |
| ADDR <5> | 15 | Address Bit-5 connected to both SRAM and ROM |
| VDD | 16 | Digital Power Supply |
| ADDR <4> | 17 | Address Bit-4 connected to both SRAM and ROM |
| ADDR <3> | 18 | Address Bit-3 connected to both SRAM and ROM |
| ADDR <2> | 19 | Address Bit-2 connected to both SRAM and ROM |
| ADDR <1> | 20 | Address Bit-1 connected to both SRAM and ROM |
| ADDR <0> | 21 | Address Bit-0 connected to both SRAM and ROM |
| DIN <0> | 22 | Data in Bit-0 connect to both SRAM and ROM |
| DIN <1> | 23 | Data in Bit-1 connect to both SRAM and ROM |
| DIN <2> | 24 | Data in Bit-2 connect to both SRAM and ROM |
| DIN <3> | 25 | Data in Bit-3 connect to both SRAM and ROM |
| DIN <4> | 26 | Data in Bit-4 connect to both SRAM and ROM |
| DIN <5> | 27 | Data in Bit-5 connect to both SRAM and ROM |
| DIN <6> | 28 | Data in Bit-6 connect to both SRAM and ROM |
| DIN <7> | 29 | Data in Bit-7 connect to both SRAM and ROM |
| DIN <8> | 30 | Data in Bit-8 connect to both SRAM and ROM |
| DIN <9> | 31 | Data in Bit-9 connect to both SRAM and ROM |
| DIN <10> | 32 | Data in Bit-10 connect to both SRAM and ROM |
| VDD | 33 | Digital Power Supply |
| DIN <11> | 34 | Data in Bit-11 connect to both SRAM and ROM |
| DIN <12> | 35 | Data in Bit-12 connect to both SRAM and ROM |
| DIN <13> | 36 | Data in Bit-13 connect to both SRAM and ROM |
| DIN <14> | 37 | Data in Bit-14 connect to both SRAM and ROM |
| DIN <15> | 38 | Data in Bit-15 connect to both SRAM and ROM |
| ROM\_CE | 39 | ROM Chip Enable |
| ROM\_OE | 40 | ROM Output Enable |
| RGB <0> | 41 | Least Significant Bit for VGA Color |
| RGB <1> | 42 | Most Significant Bit for VGA Color |
| hSync | 43 | Horizontal Sync required for VGA |
| vSync | 44 | Vertical Sync required for VGA |
| PSR <0> | 45 | Program Status Register Bit-0 used for Debugging |
| PSR <1> | 46 | Program Status Register Bit-1 used for Debugging |
| PSR <2> | 47 | Program Status Register Bit-2 used for Debugging |
| GND | 48 | Ground |
| PSR <3> | 49 | Program Status Register Bit-3 used for Debugging |
| PSR <4> | 50 | Program Status Register Bit-4 used for Debugging |
| CTRLR LATCH <1> | 51 | Controller 2 Latch signal |
| CTRLR LATCH <0> | 52 | Controller 1 Latch signal |
| CTRLR Data in <1> | 53 | Controller 2 Data Signal |
| CTRLR Data in <0> | 54 | Controller 1 Data Signal |
| CLK PULSE | 55 | Clock Output to Both Controllers |
| NC | 56 | Not Connected |
| VDD | 57 | Digital Power Supply |
| CLK | 58 | Clock Input |
| STATE BIT | 59 | Program State Bit used for Debugging |
| AUDIO DAC <0> | 60 | Audio DAC Output Bit-0 |
| AUDIO DAC <1> | 61 | Audio DAC Output Bit-1 |
| AUDIO DAC <2> | 62 | Audio DAC Output Bit-2 |
| AUDIO DAC <3> | 63 | Audio DAC Output Bit-3 |
| AUDIO\_ROM\_SPI\_MISO | 64 | Audio ROM SPI Master in Slave out |
| AUDIO\_ROM\_SPI\_MOSI | 65 | Audio ROM SPI Master out Slave in |
| AUDIO\_ROM\_SPI\_CLK | 66 | Audio rom SPI Clock |
| AUDIO\_ROM\_SPI\_CE | 67 | Audio Rom SPI Chip Enable |
| DOUT <15> | 68 | Data out Bit-15 Connected to SRAM Only |
| DOUT <14> | 69 | Data out Bit-14 Connected to SRAM Only |
| DOUT <13> | 70 | Data out Bit-13 Connected to SRAM Only |
| DOUT <12> | 71 | Data out Bit-12 Connected to SRAM Only |
| DOUT <11> | 72 | Data out Bit-11 Connected to SRAM Only |
| DOUT <10> | 73 | Data out Bit-10 Connected to SRAM Only |
| GND | 74 | Ground |
| DOUT <9> | 75 | Data out Bit-9 Connected to SRAM Only |
| DOUT <8> | 76 | Data out Bit-8 Connected to SRAM Only |
| DOUT <7> | 77 | Data out Bit-7 Connected to SRAM Only |
| DOUT <6> | 78 | Data out Bit-6 Connected to SRAM Only |
| DOUT <5> | 79 | Data out Bit-5 Connected to SRAM Only |
| DOUT <4> | 80 | Data out Bit-4 Connected to SRAM Only |
| DOUT <3> | 81 | Data out Bit-3 Connected to SRAM Only |
| DOUT <2> | 82 | Data out Bit-2 Connected to SRAM Only |
| DOUT <1> | 83 | Data out Bit-1 Connected to SRAM Only |
| DOUT <0> | 84 | Data out Bit-0 Connected to SRAM Only |

# Data path

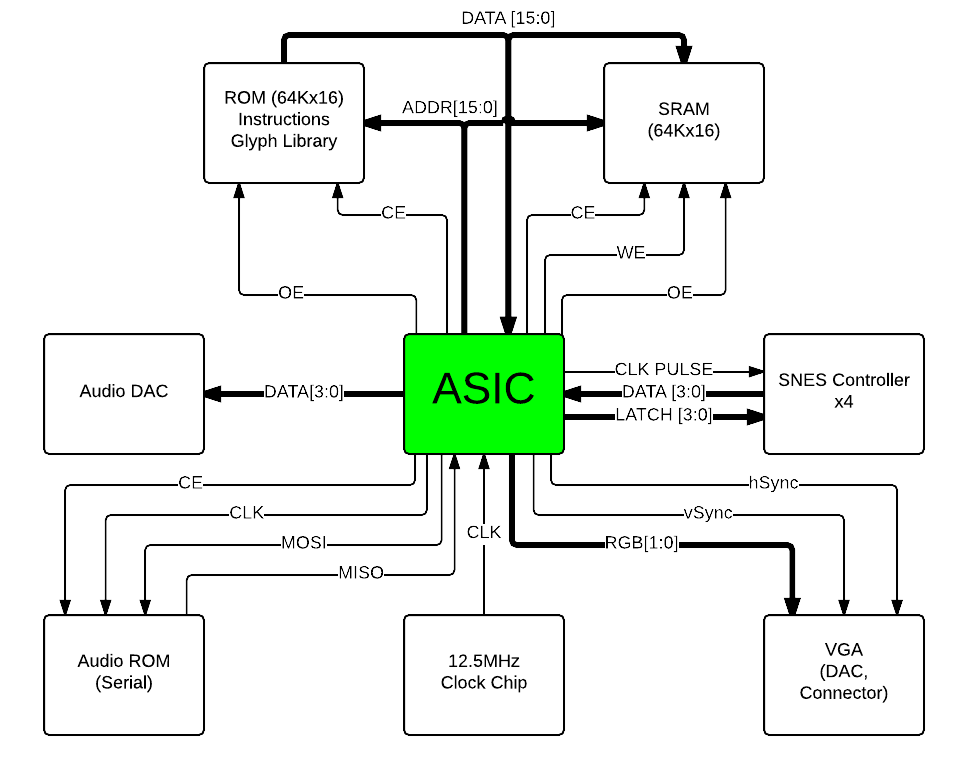
## Core

## Audio

## VGA

## Memory Map

# Peripheral interface

Application  ****

# Package Dimensions

# Verilog

This section contains the Verilog that was used to synthesize TESS.